UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/729,865	12/05/2003	En-Hsing Chen	023-0029	8494

52100 7590 02/17/2009

ZAGORIN O'BRIEN GRAHAM LLP (023)
7600B N. CAPITAL OF TEXAS HWY
SUITE 350
AUSTIN, TX 78731-1191

EXAMINER	
NGUYEN, VAN THU T	

ART UNIT	PAPER NUMBER
2824	

MAIL DATE	DELIVERY MODE
02/17/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte EN-HSING CHEN, ANDREW J. WALKER, ROY E. SCHEUERLEIN, SUCHETA NALLAMOTHU, ALPER ILKBAHAR, LUCA G. FASOLI, and JAMES M. CLEEVES

Appeal 2008-3585
Application 10/729,865
Technology Center 2800

Decided[1]: February 17, 2009

Before MAHSHID D. SAADAT, ROBERT E. NAPPI, and MARC S. HOFF, *Administrative Patent Judges*.

NAPPI, *Administrative Patent Judge.*

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 of the final rejection of claims 1, 27 and 28.[2] We have jurisdiction under 35 U.S.C. § 6(b).

---

[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 CFR § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Date (electronic delivery).

[2] Claims 2 through 20, 22, 23, and 29 through 54 were previously withdrawn from consideration. Claims 21, 24 through 26, and 55 through 60 were cancelled in the Amendment filed June 12, 2006.

We affirm the Examiner's rejection of these claims.

INVENTION

The invention is directed to semiconductor integrated circuits containing memory arrays having series-connected memory cells. *See generally* Spec. 1. Claim 1 is representative of the invention and reproduced below:

> 1. An integrated circuit comprising a memory array including memory cells arranged in a plurality of series-connected NAND strings, said memory cells comprising modifiable conductance switch devices, said NAND strings including at a first end thereof a respective plurality of series selection devices of like type, wherein each NAND string includes a second plurality of series selection devices of like type at a second end thereof, and wherein pairs of NAND strings are arranged so that:
>
> a first group of control signals couples the respective second end of one string of the pair to a global array line associated with the pair, and couples the respective first end of the other string of the pair to a respective bias node; and
>
> a second group of control signals couples the respective first end of said one string of the pair to a respective bias node, and couples the respective second end of the other string of the pair to the global array line associated with the pair.

REFERENCES

Tatsukawa	US 6,380,636 B1	Apr. 30, 2002
Sakui	US 6,411,548 B1	Jun. 25, 2002

REJECTIONS AT ISSUE

The Examiner rejected claim 1 under 35 U.S.C. § 102(b) as being anticipated by Tatsukawa.

The Examiner rejected claims 27 and 28 under 35 U.S.C. § 103(a) as being unpatentable over Tatsukawa in view of Sakui.

ISSUE

Rejection of claim 1 under 35 U.S.C. § 102(b) as being anticipated by Tatsukawa.

Appellants argue on pages 3 through 8 of the Appeal Brief and pages 1 through 3 of the Reply Brief that the Examiner's rejection of claim 1 under 35 U.S.C. § 102(b) as being anticipated by Tatsukawa is in error. Appellants argue that Tatsukawa does not disclose a plurality of series selection devices at both the first end of the NAND string and at the second end of the NAND string.

Thus, with respect to claim 1, Appellants' contentions present us with the issue: did the Examiner err in finding Tatsukawa teaches a respective plurality of series selection devices of like type at a first end of said NAND strings and a second plurality of series selection devices of like type at a second end of each NAND string?

Rejection of claims 27 and 28 under 35 U.S.C. § 103(a) as being unpatentable over Tatsukawa in view of Sakui.

Appellants argue on page 8 of the Appeal Brief and page 3 of the Reply Brief that the Examiner's rejection of claims 27 and 28 under 35 U.S.C. § 103(a) as being unpatentable over Tatsukawa in view of Sakui is in error. Appellants reason that the claims are allowable based on their dependency from claim 1. App. Br. 8.

Thus, Appellants' contentions present the same issues as presented with respect to claim 1.

FINDINGS OF FACT

1. Tatsukawa discloses the structure of a memory cell unit. Tatsukawa, col. 13, ll. 18-19 and Fig. 8.
2. Figure 8 comprises two NAND strings, connected to a main bit line, which include series selection devices and memory cells. Tatsukawa, Fig. 8.
3. On the lower portion of Figure 8, transistor SGS1 comprises a series selection device located at a first end of a NAND string. Tatsukawa, Fig. 8.
4. On the upper portion of Figure 8, transistors SGD1 and DG1 form a series of selection devices located at a second end of a first NAND string. Tatsukawa, Fig. 8.
5. On the lower portion of Figure 8, transistors SGD2 and DG3 form a series of selection devices located at a second end of a second NAND string. Tatsukawa, Fig. 8.

PRINCIPLES OF LAW

Office personnel must rely on Appellants' disclosure to properly determine the meaning of the terms used in the claims. *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 980 (Fed. Cir. 1995) (en banc). "[I]nterpreting what is *meant* by a word *in* a claim 'is not to be confused with adding an extraneous limitation appearing in the specification, which is improper.'" *In re Cruciferous Sprout Litigation,* 301 F.3d 1343, 1348, (emphasis in original) (citing *Intervet Am., Inc. v. Kee-Vet Labs., Inc.*, 887 F.2d 1050, 1053 (Fed. Cir. 1989)).

ANALYSIS

Appellants' arguments have not persuaded us of error in the Examiner's rejection of claim 1. Appellants argue that Tatsukawa does not disclose a plurality of series selection devices at both the first end of the NAND string and at the second end of the NAND string. App. Br. 3-8; and Reply Br. 1-3. Appellants agree with the Examiner that Tatsukawa teaches a plurality of series selection devices at one end of the NAND string. App. Br. 3-4. However, the Examiner has found that Tatsukawa discloses a plurality of series selection devices at both ends. Ans. 8. In addition, the Examiner has found that "claim 1 does not specifically recite any relationship to the functionality of the second selection devices with respect to the one NAND string," and therefore, "Appellants[']' arguments ar[e] based upon limitations which are not recited in claim 1." Ans. 8. We agree with the Examiner that Appellants' arguments are based upon limitations which are not recited in claim 1.

Claim 1 recites "said NAND strings including at a first end thereof a respective plurality of series selection devices of like type." Thus, claim 1 is broad enough to encompass plural selection devices for plural strings, i.e. the scope of the claims includes both: a) one selection device for the first end of each string and b) plural selection devices for the first end of each string. Claim 1 further recites "wherein each NAND string includes a second plurality of series selection devices of like type at a second end thereof." Thus, the recitation directed to the selection devices at the second end of the NAND string differs from the recitation of the selection devices at the first end, in that the claim requires that the second end of each NAND string has plural selection devices. Thus, we disagree with the Examiner's

and Appellants' interpretation that claim 1 requires a plurality of series selection devices on both ends of the NAND string. App. Br. 4-8, Ans. 5-14. While we determine that the claim is not as limited as the Examiner interprets, we find this to be harmless error as the Examiner has shown that Tatsukawa teaches the memory string as claimed.

As discussed above, we interpret claim 1 to require at least one series selection device of like type located at a first end of a NAND string and plural series selection devices of like type located on the second end of each NAND string.[3] Figure 8 in Tatsukawa shows a schematic of a memory cell unit. FF. 1. The memory cell unit comprises two NAND strings, wherein each NAND string is connected to a main bit line (MBL). FF. 2. On the lower portion of Figure 8, transistor SGS1 comprises a series selection device located at a first end of a NAND string. FF. 3. Appellants admit that SGS1 is a selection device. App. Br. 4. Therefore, as we have determined that the claim only requires one series selection device of like type located at a first end of a NAND string, we find SGS1 to meet this claim limitation.

On the upper portion of Figure 8, transistors SGD1 and DG1 form a series of selection devices located at a second end of a first NAND string. FF. 4. As noted above, Appellants admit that SGD1 and DG1 are series selection devices. App. Br. 3-4. Additionally, on the lower portion of Figure 8, transistors SGD2 and DG3 form a series of selection devices located at a second end of a second NAND string. FF. 5. Therefore, Tatsukawa discloses plural series selection devices of like type located on

[3] Claim 1 only recites the two ends of the memory string as a first end and a second end and does not recite a limitation which defines any function associated with the ends.

each NAND string. Thus, Appellants have not persuaded us that the Examiner erred in finding Tatsukawa teaches a respective plurality of series selection devices of like type at a first end of said NAND strings and a second plurality of series selection devices of like type at a second end of each NAND string as claimed. Accordingly, we sustain the Examiner's rejection of claim 1.

Rejection of claims 27 and 28 under 35 U.S.C. § 103(a) as being unpatentable over Tatsukawa in view of Sakui.

Appellants' arguments have not persuaded us of error in the Examiner's rejection of claims 27 and 28. Appellants' arguments that the rejection of these claims is in error for the reasons discussed with respect to claim 1 is not persuasive for the reasons discussed *supra* with respect to claim 1. Therefore, we sustain the Examiner's rejection of claims 27 and 28.

CONCLUSIONS OF LAW

Appellants have not shown the Examiner erred in finding that Tatsukawa discloses a respective plurality of series selection devices of like type at a first end of said NAND strings and a second plurality of series selection devices of like type at a second end of each NAND string.

SUMMARY

The Examiner's rejection of claims 1, 27 and 28 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

tdl

ZAGORIN O'BRIEN GRAHAM LLP (023)
7600 N. CAPITAL OF TEXAS HWY
SUITE 350
AUSTIN, TX 78731-1191